Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A CMOS circuit comprising:

a first gate reference voltage;

a first bias circuit source; and

a device for adjusting a current from the first bias current source to a first circuit to reduce the variation of the first circuit as a function of process, voltage and temperature, the device including:

a first transistor having a gate, a first node and a second node, ~~having its~~ the gate of the first transistor being coupled to the first gate reference voltage, ~~the device~~ the first node of the first transistor being coupled ~~in series with~~ to the first bias current source ~~and having a gate size and structure to enhance its sensitivity to process, voltage and temperature variations~~, the first transistor for generating a current sensitive to process, voltage and temperature variations;

a second transistor coupled to the first circuit and having a gate, a first node and a second node, the gate and the first node of the second transistor being coupled to the first node of the first transistor and the first bias current source, the second transistor for adjusting a current proportional to the difference between the current generated by the first bias current source and the current from the first transistor thereby compensating the current of the first bias current source for the ~~same~~ process, voltage and temperature variations.

2. (Cancelled)

3. (New) A CMOS circuit as claimed in Claim 1, wherein the structure of the gate of the first transistor includes a plurality of stripes.

4. (New) A CMOS circuit as claimed in Claim 1, wherein the first transistor and the second transistor are NMOS transistors, the first node of the first transistor being a drain, the first node of the second transistor being a drain.

5. (New) A CMOS circuit as claimed in Claim 1, wherein the first circuit includes at least one of a delay cell, a delay lock loop (DLL), a phase lock loop (PLL), a charge pump, an Operational Amplifier, and an Input/Output pad.